REMARKS

Claims 1-12 are pending in the present application. Claims 1, 4, and 8 have been amended as a result of this Response. Applicant believes that these amendments are grammatical in nature and do not limit the claims in any way. Claims 1, 4, 8, and 12 are independent claims.

ALLOWABLE SUBJECT MATTER

Applicant again acknowledges the Examiner's indication that claims 7 and 11 would be allowable if rewritten in independent form. However, Applicant respectfully submits that such an amendment is not necessary since claims 7 and 11 depend from allowable claims, for the reasons set forth below.

35 U.S.C. § 102(B) PRYOR REJECTION

Claims 1-6, 8-10 and 12 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 3,991,380 to Pryor. This rejection, in so far as it pertains to the presently pending claims, is respectfully traversed for the following reasons.

In Applicant's previous response of April 10, 2002, Applicant asserted that the signal provided at output terminal 12 of Figure 2 of Pryor is not a self bias signal, but rather an output terminal. Portions of Pryor (see e.g., Pryor, col. 4, line 52 – col. 5, line 26) make clear that the output at output terminal 12 matches the output at output terminal 22. Accordingly, Applicant argued that Pryor fails to teach a self bias signal as recited in independent claims 1, 4, 8, and 12.

In the current Office Action of September 11, 2002, the Examiner maintains the position that the signal at output terminal 12 is a self bias signal. In maintaining this assertion, the Examiner asserts that Figure 2 of Pryor teaches that an output terminal 12 is an output of the inverter 10 and also an input to a node 51, which would be considered as a self bias signal for

inverters (P5, N5 and P6, N6) in block 50 by an artisan in the art. Applicant respectfully asserts that the Examiner's position is incorrect for the following reason.

In independent claim 1 of the present application, the self bias signal is input to the gain control unit, output by the gain control unit, and utilized to control one or more other inputs to the gain control unit. Exemplary embodiments of a self bias signal are illustrated in Figures 4, 5, and 6 of the present application.

Taking Figure 6 as an example, a self bias signal O1 is produced at the drain of PMOS transistor P41. The self bias signal is output from the gain control circuit (which includes PMOS transistors P42B and P43B and NMOS transistors N42B and N43B). The self bias signal O1 is utilized to control a second input to the gain control circuit at node N1. Applicant respectfully submits that there is no circuitry in Figure 2 of Pryor to which the signal at output terminal 12 is input to and from which the signal at output terminal 12 is output and utilized to control a second input to that same circuitry. In the absence of such circuitry, Applicant reiterates his position that the signal at output terminal 12 is not a self bias signal. Accordingly, Applicant respectfully submits that independent claim 1 is allowable over Pryor for at least this reason.

Applicant respectfully submits that independent claims 4, 8, and 12 are allowable over Pryor for similar reasons. Applicant also respectfully submits that dependent claims 2-3, 5-6, and 9-10 are allowable over Pryor by virtue of their dependency on allowable independent claims 1, 4, or 8.

Further, with respect to claims 2, 5, and 9, in Applicant's prior response of April 10, 2002, Applicant's argued that P5, P6, N5, N6 shown in Figure 2 of Pryor do not describe a gain control unit, as recited in Applicant's claims 2, 5 and 9.

In response, in the current Office Action, the Examiner has maintained this rejection again relying on transistors P5, N5, P6, and N6 of Figure 2 of Pryor. Applicant again respectfully submits that the four transistors relied upon by the Examiner in Figure 2 of Pryor (or any other arrangement of circuitry in Pryor) do not teach a gain control unit including cross coupled transistors, as recited in dependent claims 2, 5, and 9. For example, the Examiner asserts that transistor P5 corresponds to the first PMOS transistor of dependent claim 2. However, as recited in independent claim 2, the first PMOS transistor has its drain connected to the self bias signal. As clearly illustrated in Figure 2, the gate of transistor P5 is connected to the Examiner's alleged self bias signal (the signal at output terminal 12). Applicant respectfully submits that this is merely one example of the differences between dependent claims 2, 5 and 9 and transistors P5, N5, P6, and N6 of Figure 2 of Pryor. Applicant respectfully submits that dependent claims 2, 5 and 9 are allowable over Pryor, for at least this additional reason.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the rejections and allowance of each of claims 1-12 is respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any

additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By 45,224
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MARKED UP VERSION OF THE CLAIMS

1. (Amended) An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias singal;

a second inverting switch connected to a second input voltage and outputting an output signal;

a gain control unit having a feedback loop for gain control and responding to the self bias signal and the output signal.

4. (Amended) An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting [a] an output signal;

a gain control unit having a feedback loop for gain control responsive to the self bias signal and the output signal; and

a current controlling circuit that supplies current to the first inverting switch, the second inverting switch and the gain control unit and sinks current from the first inverting switch, the second inverting switch and the gain control unit, the current controlling circuit responding to the self bias signal.

8. (Amended) An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting [a] an ouput signal;

a gain control unit having a feedback loop for gain control responsive to the self bias signal and the output signal; and

a swing width control circuit connected to a feedback signal that is inverted by the output signal.